AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0021] as follows:

[0021] FIG. 1 illustrates a multiprocessor system ~~in accordance with an embodiment of the present invention~~.

Please add the following new paragraph after paragraph [0024]:

[0025] FIG. 4 is a flowchart illustrating the process for facilitating cache coherence with adaptive write updates in accordance with an embodiment of the present invention.

Please add the following new paragraph after paragraph [0030]:

[0030.5] The process of implementing cache coherence with adaptive write updates is summarized as follows: The system starts by initializing the cache to operate using a write-invalidate protocol. During program execution, the system monitors the dynamic behavior of the cache. If the dynamic behavior indicates that better performance can be achieved using a write-broadcast protocol, the system switches the cache to operate using the write-broadcast protocol. In addition, the system may enable locking the cache to operate only under the write-invalidate mode in a shared-memory multiprocessor system in which caches are unable to switch into the write-broadcast mode.

Please add the following paragraph after paragraph [0047]:

[0048] FIG. 4 is a flowchart illustrating the process for facilitating cache coherence with adaptive write updates in accordance with an embodiment of the present invention. The system starts when the cache 161 is initialized to operate using the write invalidate protocol (step 402). Next, the dynamic behavior of the cache 161 is monitored by counting the cache line invalidations (step 404). This

count is checked against a threshold (step 406). If the number of cache line invalidations is not above a certain threshold, then the cache operates using the write invalidate protocol (step 410). If the threshold is exceeded, then in one embodiment of the invention, if the cache is able to switch to operate using the write broadcast (step 408), then the cache is switched to the write broadcast protocol (step 412), otherwise the cache is switched to the write invalidate protocol (step 410).